Amendments to the Claims:

Please cancel claims 1-6, 9, 11 and 12.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1.-6. (Cancelled)

7. (Currently Amended) A control signal generation circuit comprising:

a first latch which latches an input signal in response to a clock signal and outputs an output signal to a first output of the control signal generator and to an input terminal of a second latch;

[[a]]the second latch which latches [[an]]the output signal of the first latch in response to the clock signal;

a third latch which latches an output signal of the second latch in response to the clock signal; and

a selection circuit which outputs one of the output signal of the second latch and an output signal of the third latch in response to a test enable signal to a second output of the control signal generator,

wherein:

the amount of time from when the output signal of the first latch is activated to when an output signal of the selection circuit is activated is controlled in units of bit time of the clock signal,

the output signal of the first latch is a column latch signal,

the output signal of the selection circuit is a data input/output command signal, and

the column latch signal is a control signal coupled between the control signal generation circuit and a memory circuit and used to latch a column address for accessing the memory circuit, and the data input/output command signal is a control signal coupled between the control signal

generation circuit and the memory circuit and used to control data read and write operations on a selected column of the memory circuit.

8. (Currently Amended) The control signal generation circuit of claim 7 comprising:

a first inverter which inverts the output signal of the first latch;

a second inverter which is connected between an output terminal of the first latch and [[an]]the input terminal of the second latch; and

a third inverter which is connected between an output terminal of the second latch and an input terminal of the third latch,

wherein the selection circuit has a first input terminal connected to an output terminal of the third latch and a second input terminal connected to the output terminal of the second latch.

9. (Cancelled)

10. (Original) The control signal generation circuit of claim 7, wherein the output signal of the first latch is an inverted signal of the input signal.

11.-12. (Cancelled)